

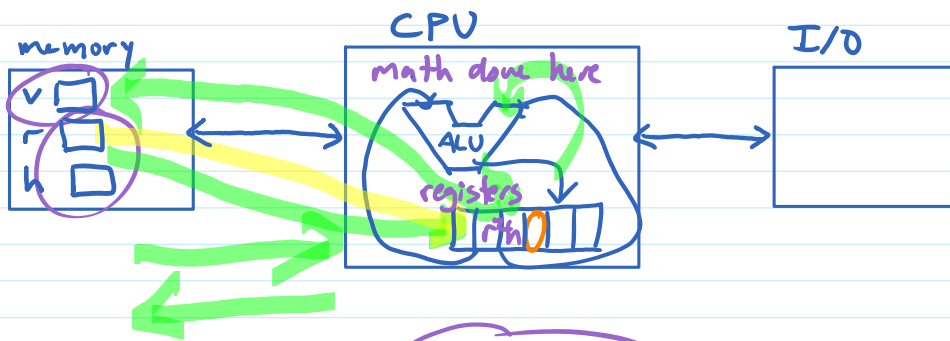
Source Code Translation



CPU: Qualcomm Snapdragon 845

CPU : Intel Core i5 6300U

von Neumann architecture



CPU 1

load r into register 1
 mult r1 by r1 result → r1
 load h into r2
 r1 * r2 → r3
 load pi into r4
 r3 * r4 → r0
 store r0 into v

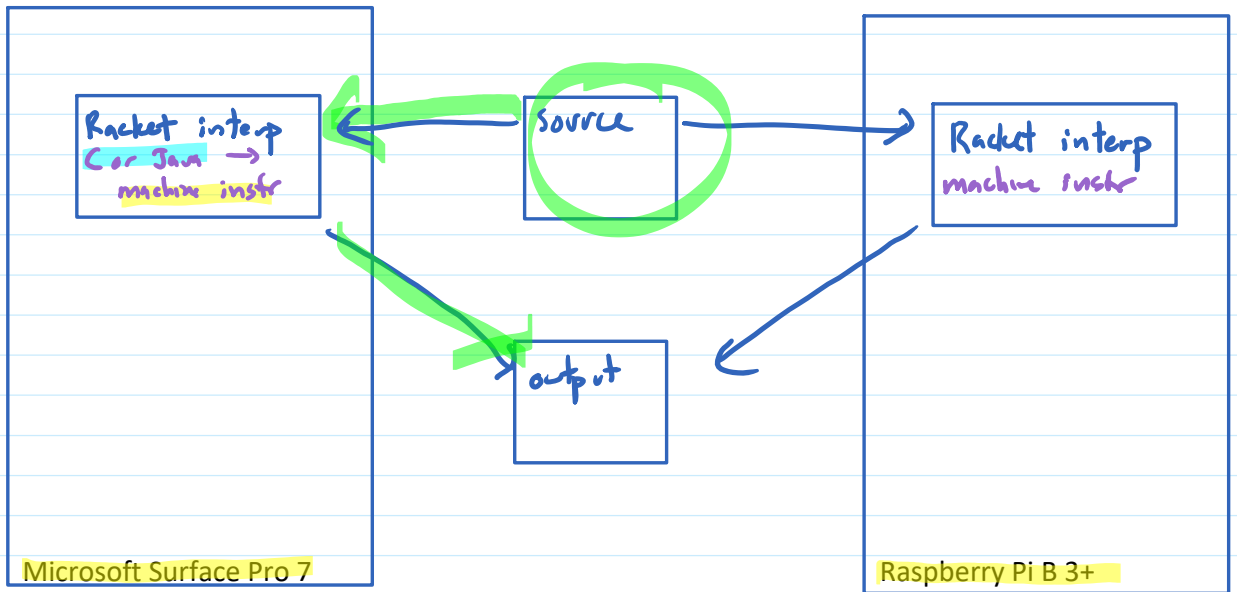
CPU2

load r into r1
 square r1 r² in r1
 load h into r2
 mult r1, r2 h * r² in r2
 mult-pi r2 π * r² * h in r2
 store r2 in v

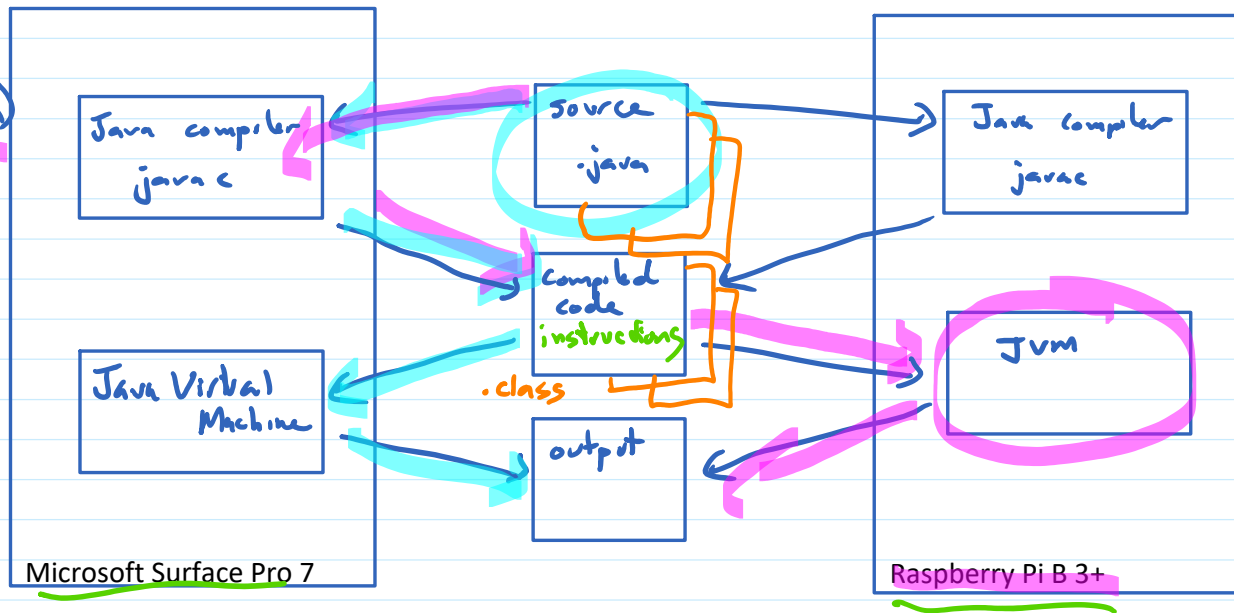
Interpreters vs Compilers

Interpreter

Racket



Java
C++
Python (implementation)



C

